

REMARKS

By the above amendment, independent claims 13 - 15 and 18 have been amended to clarify features of the present invention and the dependent claims have been amended in accordance therewith as well as in a manner to overcome the rejection of such claims under 35 USC 112, second paragraph. Additionally, the specification has been amended in the manner suggested by the Examiner and new dependent claims 21 - 24 have been presented.

With regard to the rejection of claims 16 and 19 under 35 USC 112, second paragraph, by the present amendment, such claims have been amended in a manner which is considered to be compliance with 35 USC 112, second paragraph. For example, claim 16 has been amended to depend from claim 14 or 15 and now recites the feature that the clip circuit, as recited in claims 14 and 15 have a structure as recited and operates so that an absolute volume of the voltage increases with time. Furthermore, claim 19 has been retained without amendment present claim 18 has been amended to recite "a" duty ratio, and thereby provide of antecedent basis for "the" duty ratio of claim 19. Thus, claims 16 and 19 should be considered to be in compliance with 35 USC 112, second paragraph.

With regard to the amended claims, it is noted that claim 13 has been amended to recite the feature that the plasma processing method flattens a voltage waveform of a high frequency voltage supplied by the wafer bias power generator to a voltage that varies in an inclined manner with time and flattens either a positive side voltage or a negative side voltage of the voltage wave form at an arbitrary voltage. That is, in accordance with the present invention, a clip circuit as illustrated in Figures 2 - 4, for example, effects clipping of the high frequency voltage of the wafer bias power source 117 so as to provide a voltage waveform in which a positive

side voltage or a negative side voltage is flattened so as to provide a voltage that varies in an inclined manner with time, with Fig. 5 illustrated the clipping or flattening of the voltage waveform of a sine wave with the frequency of 400 kHz at a arbitrary voltage and controlling the inclination of the flat portion on the negative side voltage, which feature is also illustrated in Fig. 7 of the drawings of this application and which is now recited in claim 13 and the dependent claims thereof.

It is noted that claim 14 recites the feature that the plasma processing method clips at least either a positive side voltage or a negative side voltage of a high frequency voltage of the wafer bias generator to a predetermined voltage by using means for flattening the high frequency voltage which includes a clip circuit connected to the wafer bias power generator.

Claim 15 recites the feature that the plasma processing method clips at least either a positive side voltage or a negative side voltage of a high frequency voltage of the wafer bias power generator to a voltage that varies in an inclined manner with time by using means for flattening the high frequency voltage which includes clip circuit connected to the wafer bias power generator.

Newly added dependent claim 21 which depends from claims 13 - 15 further defines the high frequency voltage as being a sine wave with new dependent claim 22 which depends from claim 13 reciting the features of the sine wave and means for clipping thereof.

Independent claim 18 recites the feature of the plasma processing method flattening a rectangular voltage waveform of a high frequency voltage to a voltage that varies in an inclined manner with time for at least one of a positive side voltage and a negative side voltage and applying the high frequency voltage with a predetermined duty ratio to the object to be processed so that a high frequency

voltage waveform generated at the object is substantially rectangular. As illustrated in Fig. 16, the substantially rectangular input waveform, by way of the waveform controller 12 of Fig. 15, is clipped at an arbitrary voltage both at the positive voltage and the negative voltage sides so that the waveform is changed from a flat-clipped waveform to a waveform where the absolute value increases with time on both the positive and negative sides with the duty ratio also being controlled in the manner described and improvements in etching being obtained. It is noted that with such waveform, a waveform of the high frequency voltage at the wafer is obtained as illustrated in Fig. 17, and Figs. 16 and 17 are contrasted with Figs. 19 and 20, in which a rectangular high frequency voltage is applied to the wafer mounting electrode 9 resulting in a waveform of the high frequency voltage at the wafer, as shown in Fig. 20 wherein the ion energy distribution becomes broad, with the width of the high energy peak and low energy peak increased and peak ion flux decrease. Therefore, as described in the first full paragraph at page 30 of the specification, the etching rate, the process accuracy and the material selectively all drop in accordance with Figs. 19 and 20, which is avoided with the present invention. That is, as described in the last paragraph of page 30, by applying to the wafer mounting electrode 9 of voltage having a waveform that switches between positive voltage and negative voltage with the absolute value increasing with time, to thereby create a rectangular high frequency voltage at the wafer, a highly accurate and efficient etching is made possible and the selectively of the material is improved, as obtained with the present invention.

Applicants submit that these features are now recited in the independent and dependent claims of this application and such features are not disclosed or taught in the cited art as will become clear from the following discussion.

As to the rejection of claim 13 under the judicially created doctrine of obviousness-type double patenting, as being unpatentable over claims 1 - 3 of US Patent No. 6,806,201 (Sumiya et al) in view of Tomoyasu et al (5,900,103), this rejection is traversed insofar as it is applicable to claim 13, as amended.

As noted above, claim 13 recites the feature that a voltage waveform of a high frequency voltage supplied by the wafer bias power generator is flattened to a voltage that varies in an inclined manner with time and flattens either a positive side voltage or a negative side voltage at an arbitrary voltage. While claims 1 - 3 of Sumiya et al described flattening of the positive voltage side and negative side voltage of the RF bias voltage as illustrated in Fig. 12, for example, it is readily apparent that the flattened portion of Sumiya et al is not "a voltage that varies in an inclined manner with time" and applicants submit that it cannot be considered obvious from the claimed invention of Sumiya et al to provide such features. Furthermore, irrespective of the disclosure of Tomoyasu et al, applicants submit that this patent also fails to disclose or teach the flattening of the voltage waveform of a high frequency voltage to a voltage that varies in an inclined manner with time at either a positive side voltage or a negative side voltage. Thus, applicants submit that Tomoyasu et al in combination with Sumiya et al (US Patent 6,806,201) fails to provide the claimed features of claim 13 such that the obviousness-type double patenting rejection as set forth by the Examiner is improper and should be overcome.

As to the rejection of claims 13 - 14, 17 - 20 under 35 USC 102(b) as being anticipated by Arai et al (6,110,287) the rejection of claims 13 and 14 under 35 USC 102(e) as being anticipated by Quon et al (US Patent Application Publication No. 2003/0094239 A1); and the rejection of claims 15 and 16 under 35 USC 103(a) as

being unpatentable over Quon et al (US Patent Application Publication No. 2003/0094239 A1) in view of Kaji et al (US Patent No. 6,129,806), such rejections are traversed insofar as they are applicable to the present claims and reconsideration and withdrawal of the rejections are respectfully requested.

As to the requirements to support a rejection under 35 USC 102, reference is made to the decision of In re Robertson, 49 USPQ 2d 1949 (Fed. Cir. 1999), wherein the court pointed out that anticipation under 35 U.S.C. §102 requires that each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. As noted by the court, if the prior art reference does not expressly set forth a particular element of the claim, that reference still may anticipate if the element is "inherent" in its disclosure. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Moreover, the court pointed out that inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.

As to the requirements to support a rejection under 35 USC 103, reference is made to the decision of In re Fine, 5 USPQ 2d 1596 (Fed. Cir. 1988), wherein the court pointed out that the PTO has the burden under '103 to establish a prima facie case of obviousness and can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. As noted by the court, whether a particular combination might be "obvious to try" is not a legitimate test of patentability and obviousness cannot be

established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. As further noted by the court, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.

Furthermore, such requirements have been clarified in the recent decision of In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002) wherein the court in reversing an obviousness rejection indicated that deficiencies of the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge".

The court pointed out:

The Examiner's conclusory statements that "the demonstration mode is just a programmable feature which can be used in many different device[s] for providing automatic introduction by adding the proper programming software" and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial" do not adequately address the issue of motivation to combine. This factual question of motivation is immaterial to patentability, and could not be resolved on subjected belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher."... Thus, the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion. (emphasis added)

Turning to Arai et al, while the Examiner contends that this patent discloses applying a bias voltage to a substrate electrode (55) which power is modulated with time in the form of a rectangular wave (see, col. 9, line 66 to col. 10, line 2 and Figs. 3 and 8) and flattening the voltage of the square wave through the use of an amplitude modulator, applicants submit that Arai et al does not disclose flattening a voltage waveform of a high frequency voltage supplied from the wafer bias power

generator to a voltage that varies in an inclined manner time and flattens either a positive side voltage, as recited in claim 13, clips at least either a positive side voltage or negative side voltage of a high frequency voltage of the wafer bias voltage generator to a predetermined voltage by using means for flattening the high frequency voltage which includes a clip circuit connected to the wafer bias power generator, as recited in claim 14, or flattens a rectangular voltage waveform of a high frequency voltage to a voltage that varies in an inclined manner with time for at least one of a positive side voltage and a negative side voltage, as recited in claim 18, in the sense of 35 USC 102 or 35 USC 103. Applicants note that while Arai et al discloses combining different waves to obtain different waveforms as illustrated in Figs. 6, 8, 10 and 12 of this patent. With respect to the rectangular waveform of Fig. 8, for example, as described in column 9, lines 62 to 67, such waveform is obtained by combination of the oscillators G1, G3, G5 and G7 so that only waves with an odd-number of times of frequency of the basic wave is oscillated and synthesized resulting in the waveform, and does not provide for flattening of the waveform, and in particular, flattening of a waveform to a voltage that varies in an inclined manner with time on either the positive side or negative side. Thus, applicants submit that the independent and dependent claims of this application patentably distinguish over Arai et al in the sense of 35 USC 102 and 35 USC 103 and should be considered allowable thereover.

As to the rejection of claims 13 and 14 as being anticipated by Quon et al, as noted above, claim 13 recites the feature of flattening a voltage waveform of a high frequency voltage supplied by the wafer bias power generator to a voltage that varies in an inclined manner with time. Irrespective of the Examiner's contentions, the publication of Quon et al merely discloses that an RF voltage source produces a

relatively low frequency RF voltage and a VHF voltage source produces a VHF voltage having a higher frequency than the RF voltage, and a coupling circuit combines the RF and the VHF voltages. More particularly, a combiner circuit 34 adds or superposes the respective RF and VHF signals which are then filtered. It is readily apparent that Quon et al does not disclose or teach the flattening of the voltage waveform of a high frequency voltage supplied by the wafer bias power generator to a voltage that varies in an inclined manner with time, as recited in claim 13 or which clips either a positive side voltage or a negative side voltage of a high frequency voltage of the wafer bias power generator to a predetermined voltage by using means for flattening the high frequency voltage which includes a clip circuit connected to the wafer bias power generator. Irrespective of the Examiner's contentions, the coupling circuit 12 of Quon et al is not a clip circuit connected to the wafer bias power generator, in the manner set forth. Thus, applicants submit that claims 13 and 14, as amended, patentably distinguish over Quon et al in the sense of 35 USC 102 and should be considered allowable thereover.

As to the application of Quon et al in combination with Kaji et al with respect to the features of claims 15 and 16, the Examiner recognizes that Quon et al fail to teach the voltage varies in an inclined manner with time. The Examiner however, refers to Kaji et al as teaching a plasma processing apparatus comprising an electrostatic wafer electrode 15 and a bias voltage source wherein the bias voltage pulse and may have an inclined portion shown in Figs. 7 and 8. Therefore, the Examiner contends that it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the pulse generator mechanism including an inclined waveform as taught by Kaji et al in the process of Quon et al. Applicants submit the Examiner has engaged in a hindsight reconstruction attempt utilizing the

principle of "obvious to try" which is not the standard of 35 USC 103. See, In re Fine, supra. Moreover, applicants submit that the utilization of a pulsed bias voltage as disclosed by Kaji et al differs from the utilization of a low frequency and high frequency voltage addition or superposition as described in Quon et al, and represents a hindsight reconstruction attempt. In this regard, it is noted that Kaji et al was available to Quon et al prior to the invention of Quon et al, and it is apparent that Quon et al did not adopt the teachings of Kaji et al therein, which is evidence of a hindsight reconstruction attempt. Additionally, Kaji et al does not disclose or teach clipping at least either a positive side voltage or a negative side voltage of a high frequency voltage of a wafer bias power generator to a voltage that varies in an inclined manner with time by using means for flattening the high frequency voltage which includes a clip circuit connected to the wafer bias power generator, as recited in claim 15, which feature is also not disclosed by Quon et al. As to dependent claim 16, irrespective of the contentions by the Examiner, neither Quon et al nor Kaji et al discloses a clip circuit which comprises a diode and a DC voltage unit that are mutually connected in series, controlling the voltage of the DC voltage unit so that an absolute volume of the voltage increases with time. As such, applicants submit that claims 15 and 16 patentably distinguish over this proposed combination of references in the sense of 35 USC 103 and should be considered allowable thereover.

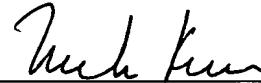
For the foregoing reasons, favorable action in this application is requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli,

Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 648.42465CX1),
and please credit any excess fees to such deposit account.

Respectfully submitted,

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